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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,567	03/12/2004	Toguto Maruko	SAT 199	6520

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,567	MARUKO, TOGUTO	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 11 October 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,4-5 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (U.S. Patent 5,729,894).

Rostoker discloses a ball grid array (Fig. 12) that contains a plurality of connection terminals (520) to be connected to a wiring on the board (506) and a plurality of test terminals (520d/e) on a joint surface thereof to said board, where the test terminals are electrically isolated from the wiring and wherein a first area where said connection terminals are arranged at predetermined pitches in a lattice and a second area where said test terminals are arranged at pitches narrower than said predetermined pitches in a lattice are placed, where the connection and test terminals are solder balls and has a semiconductor package mounted on the board.

The second area is placed in the center of the joint surface and first area is placed in the periphery of joint surface so as to surround the second area

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1,2,4-5,7-12 and 22-23 are rejected under 35 U.S.C. 102(a) as being anticipated by Ando (JPO 2000-068403).

Ando discloses a ball grid array (Abstract) that contains a plurality of connection terminals (14) to be connected to a wiring on the board (11a) and a plurality of test terminals (13) on a joint surface thereof to said board, where the test terminals are electrically isolated from the wiring and wherein a first area where said connection terminals are arranged at predetermined pitches in a lattice and a second area where said test terminals are arranged at pitches narrower than said predetermined pitches in a lattice are placed, where the connection and test terminals are solder balls and has a semiconductor package mounted on the board

The second area is placed in the center of the joint surface and first area is placed in the periphery of joint surface so as to surround the second area

The second area is placed in the periphery and first area surrounds the first area.

The second area is placed on a high heat buildup circuit since the second area is used for heat radiation (Abstract)

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3,7-9,13-18 and 22-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (U.S. Patent 6,815,621).

Park discloses a chip scale package (Figs. 16 and 17) that contains a plurality of connection terminals (52) to be connected to a wiring on the board and a plurality of test terminals (53) on a joint surface thereof to said board, where the test terminals are electrically isolated from the wiring and wherein a first area where said connection terminals are arranged at predetermined pitches in a lattice and a second area where said test terminals are arranged at pitches narrower than said and has a semiconductor package mounted on the board predetermined pitches in a lattice are placed, where the connection and test terminals are solder balls and lands (Fig. 17 (58/59)) and can be mounted to ground (Column 1, lines 54-61)

The second area is placed in the periphery of joint surface and first area is placed to surround the second area

The first area is formed at a plurality of places and second area is placed so to isolate first area in the plurality of places

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of Park.

Rostoker discloses all the limitations except for the terminals to be lands. Whereas Park discloses a chip scale package (Fig. 17) with connection terminals (58) and test terminals (59) where the connection terminals have a first pitch and the test terminals have a second pitch and the terminals are lands. The connection terminals and test terminals are lands for connection of signal lines to the lands in the adjacent row/column. (Abstract) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Rostoker by incorporating the connection and test terminals to be land for connection of signals lines as taught by Park.

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Park.

Ando discloses all the limitations except for the terminals to be lands. Whereas Park discloses a chip scale package (Fig. 17) with connection terminals (58) and test terminals (59) where the connection terminals have a first pitch and the test terminals have a second pitch and the terminals are lands. The connection terminals and test terminals are lands for connection of signal lines to the lands in the adjacent row/column. (Abstract) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Ando by

incorporating the connection and test terminals to be land for connection of signals lines as taught by Park.

Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker.

Rostoker discloses all the limitations except for the second area to be placed in the four corners of the surface and the first area is placed in an area except for four corners. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the second area to be placed in the four corners of the surface and the first area is placed in an area except for four corners, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70 (1950).

Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando.

Ando discloses all the limitations except for the second area to be placed in the four corners of the surface and the first area is placed in an area except for four corners. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the second area to be placed in the four corners of the surface and the first area is placed in an area except for four corners, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70 (1950).

Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park.

Park discloses all the limitations except for the second area to be placed in the four corners of the surface and the first area is placed in an area except for four corners. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the second area to be placed in the four corners of the surface and the first area is placed in an area except for four corners, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70 (1950).

Response to Arguments

Applicant's arguments filed 11 October 2005 have been fully considered but they are not persuasive. Applicant argues that the Rostoker, Ando or Park reference disclose test terminals this is erroneous since all the reference disclose the structural limitations of the claimed invention and in addition the test terminals (solder balls) that are formed in the central area that have a smaller pitch then the connection terminals surrounding the test terminals are not electrically connected to the test terminals and are electrically independent from the connection terminals and can be used as a test terminals. In addition, even though the solder balls (test terminals) are used to dissipate heat all solder balls are used for that purpose and does not mean that it cannot be used as a test terminal. Therefore the rejection stands.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

ZANDRA V. SMITH
SUPERVISORY PATENT EXAMINER
9 January 2006